		i			Ш												
•	М	4.	-	1	7	8	**	0	0 :	\$ -	ũ	0 1	5	5	0 3	5	*

ML-178-003-003203 Seat No.\_

B. C. A. (Sem. II) (CBCS) Examination April/May - 2012

CS - 09 : Computer Organization & Architecture

Faculty Code: 003 Subject Code: 003203

Time :  $2\frac{1}{2}$  Hours]

[Total Marks: 70

## SECTION - I

1	MC	Q.		20
	(1)	The	control and arithmetic logic sections are called	
		(A)	Block diagram	
		(B)	Control unit	
		(C)	Input/output unit	
		(D)	Central processing unit	
	(2)	Soft	tware interrupt is in initiated by	
		(A)	Signal	
		(B)	Wave form	
		(C)	Executing an instruction	
		(D)	None	
	(3)	Stac	ck means	
		(A)	FIFO	
		(B)	LIFO	
		(C)	LICO	
		(D)	None	
ML-	178-	003-0	003203] 1 [Co	ntd

(4)	The	memory bus is made up of two parts	and
	(A)	Data bus, address bus	
	(B)	RAM, ROM	
	(C)	Data bus, RAM	
	(D)	Buffer, address bus	
(5)		address register is after each word	that is
	(A)	Decremented	
	(B)	Incremented	
	(C)	Null	
	(D)	Can't be decided	
(6)		en BR input is active, the CPU the en ecurrent instruction and places the address	
	(A)	Start	
	(B)	Terminates	
	(C)	Suspend	
	(D)	None of the above	
(7)		decoders presented in the section are called decoder, where m	n-to-m
	(A)	=2 <sup>n</sup>	
	<b>(B)</b>	>=2 <sup>n</sup>	
	(C)	<=2 <sup>n</sup>	
	(D)	>2 <sup>n</sup>	
(8)	1011	1001110 + 101 =	
	(A)	1001111	
	<b>(B)</b>	10001111	
	(C)	10001110	
	(D)	10011110	
ML-178-0	03-0	03203] 2	[Contd

(9)	When inputs J and K are both equal to 1, a clock transition switches the outputs of the flip flop to their
	state.
	(A) No change
	(B) Clear to 0
	(C) Set to 1
	(D) Complement
(10)	The behavior of a sequential circuit is determined from the inputs, the outputs and the
	(A) Present state
	(B) State of its flip flops
	(C) Next state
	(D) None of the above
(11)	A 2 <sup>n</sup> to 1 multiplexer has input data lines and input selection lines.
	(A) n,2 <sup>n</sup>
	(B) 1, 2 <sup>n</sup>
	(C) 2, 2 <sup>n</sup>
	(D) 2 <sup>n</sup> , n
(12)	A telephone dial system is an example of
	circuit.
	(A) Asynchronous
	(B) Synchronous
	(C) Combinational
	(D) Sequential
(13)	In full adder, there are input and output terminal.
	(A) Two, two
	(B) Three, two
	(C) Two, three
	(D) None of the above
ML-178-0	003-003203] 3 [Contd

(14)		input of half adde	er is 1 0 0 then o	utput of sum bit	-
	(A)				
	(B))				
		Can't determine			
	(D)	Invalid number of	finputs		
(15)		transfer of new in		register is	
	(A)	Expanding			
	(B)	Starting			
	(C)	Loading			
	(D)	Ending			
(16)		output of sequentits as well as			
	(A)	Present, previous			
	(B)	Previous, present			
	(C)	Complement, pres	ent		
	(D)	Previous, complem	ent		
(17)		input of full adde	r is 1 0 1 then ou	atput of carry bit	
	(A)				
	(B)				
	(C)	Invalid number of	innuta		
		ultiplexer is also k	-		
		Coder	nown as		
	(B)	Decoder			
		Data selector			
	, ,	Multi vibrator			
ML-178-0			4	[Contd	

	capable of storing one bit of in formation.  (A) Gates
	(B) IC
	(C) Clock pulses
	(D) Flip flop
(20	0) 110010101*1001 =
	(A) 110000111101
	(B) 111000111100
	(C) 111100111100
	(D) 111000111101
	SECTION - II
1 (a)	Attempt any three :
	<ol> <li>What is logic gate? Explain AND, OR, NOT gate with truth table.</li> </ol>
	(2) What is don't care condition? Explain with example.
	(3) Reduce following Boolean expression.
	(a) (BC'+A'D)(AB'+CD')
	(b) AB+A(CD+CD')
	(4) Write a short note on ALU.
	(5) What is parity bit ? Explain.
	<ul><li>(5) What is parity bit ? Explain.</li><li>(6) Construct a full adder using two half address.</li></ul>
(b)	
(b)	(6) Construct a full adder using two half address.
(b)	(6) Construct a full adder using two half address.  Attempt any three:
(b)	<ul><li>(6) Construct a full adder using two half address.</li><li>Attempt any three:</li><li>(1) Write a short note on unidirectional shift register.</li></ul>

Give difference between combinational circuit and sequential circuit (4) Explain fixed point representation. (5) Explain input output processor. Write a short note on asynchronous serial transfer. 10 Attempt any two: (1) What is Flip Flop? Explain with types. (2) Explain register with parallel load. (3) What is combinational circuit? Explain with types. (4) Write a short note on asynchronous data tranfer. What is DMA? Explain DMA controller. Attempt any three: 6 (1) Write a short note on modes of data transfer. (2) Explain accumulator register. (3) Explain different addressing modes. (4) Discuss NAND gate as a universal gate. (5) Convert into reverse polish notation. (A\*B)/[(C\*D)+E\*F](6) Prove following Boolean algebra (a) AB+A(B+C)+B(B+C)=B+AC. (b) (X+Y')(X'+Y) = XY+X'Y'(b) Attempt any three: 9 (1) What is interrupt? Explain types of interrupt. (2) Write a short note on DMA transfer. (3) Explain CPU - IOP communication with chart. ML-178-003-003203] [Contd...

(c)

- (4) Write a short note on counter.
- (5) Explain octal to binary encoder in detail.
- (6) Write short note on IOP>
- (c) Attempt any two:

10

- (1) Explain general register organization.
- (2) Explain register stack with push and pop algorithm.
- (3) Explain Instruction ? Formats with types.
- (4) What is decoder. Explain 3 to 8 line decoder in detail.
- (5) Write a short note on multiplexer.

ML-178-003-003203]

7

[ 7400/230-50 ]